REMARKS

I. Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a), asserting that the drawings failed to show features as described in the specification. The Examiner argued that any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. The Examiner stated that a proposed drawing correction or corrected drawings are required in reply to the Office Action to avoid abandonment of the application.

The Examiner requested that the Applicant revise the drawings without adding any new material. The Examiner also indicated that any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. The Examiner cited the following items which require revision.

Regarding Figs. 1-15, the Examiner stated that the gate oxide over which the DRAM poly gate is formed and semiconductor substrate in which STI is formed are not shown. The Applicant has revised the drawings, which are included, herewith, to show both the gate oxide and the substrate. Applicant asserts that this issue has now been removed.

Regarding Figs. 2-15, the Examiner stated that LDD is not indicated. The Applicant asserts that LDD is shown. The Applicant refers the Examiner to Fig. 7, which shows "LDD". Note that it is not necessary to show LDD until Fig. 7, because in the steps prior to Fig. 7 (i.e., Figs. 1-6), LDD is not an issue at that point with regard to the fabrication processes. Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 3, the Examiner argued that an IPO-1 and plug ion implant are now shown. Applicant has modified Fig. 3 so that IPO planarization is shown. Applicant points out, however, that any plug ion implant is implied because of the presence of 34, 36, and 38. Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 6, the Examiner argued that the SiON layer is not indicated. Applicant points out that Fig. 6 shows a step after SiON was removed. SiON appears in Fig. 5, which has modified to indicate SiON. It can be surmised from the drawings that SiON was added after Fig. 4 and removed after Fig. 5, but prior to the step shown in Fig. 6. Therefore, Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 8, the Examiner argued that the outline of the resist is not shown and that the location of the resist is not clear. Applicant has modified Fig. 8 to point out the resist and its location. Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 9, the Examiner stated that it is not clear as to what material is left after dry etching of TEOS. Examiner also indicated that the outline of the resist is not shown in Fig. 9. Applicant points out to the Examiner that it is not necessary to show what material is left after dry etching of TEOS, because the specification points out that Fig. 9 shows the results of a space TEOS dry etch. This is sufficient enablement for one skilled in the art to understand the overall fabrication steps of Applicant's invention. Additionally, Applicant has identified resist in Fig. 9 show it is not necessary to show the outline (i.e., see Fig. 7). Therefore, Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 10, the Examiner stated that space TEOS is not shown. Applicant points out that it is not necessary to show a space TEOS, because the

specification clearly points out that Fig. 10 shows the results of a TEOS wet dip. Also, TEOS is discussed thoroughly with respect to Fig. 17. The figures in their totality, including the specification and background provide sufficient enablement thereof. Applicant therefore asserts that this issue has now been removed.

Regarding Figs. 10-15, the Examiner stated that it is not clear what is the material on 34, 36, and 38. The Applicant asserts that it is clear that a resist material is located on 34, 36, and 38 at various stages in the processes of Figs. 10-15. Therefore, Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 12, the Examiner stated that it is not clear whether S/D implant is done only in the DRAM area. Applicant respectfully disagrees with this assessment. The box labeled "N+S/D Implant" is located sufficiently above the substrate and components thereof to indicate that the implant operation occurs across the entire top thereof. Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 13, the Examiner stated that it is not clear where Cobalt silicide is formed with respect to doped polysilicon and that additionally, the location of silicon nitride space 92 is not clear. Applicant has corrected Fig. 13 to show that 92 surrounds 34, 36, and 38. Applicant also submits that it is clear that Co-Salicide is formed on the "black" areas shown by the reference numeral 90. Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 14, the Examiner argued that it is not clear where SiON is formed. In Fig. 14, SiON is shown formed on the black areas thereof. It is clear from Figs. 13 and 14 that the flow involves layering thereof. Also, Applicant suggests that the Examiner review the text in addition to the drawings, because the text of the detailed description also enables the claims. Applicant therefore asserts that this issue has now been removed.

Regarding Fig. 15, the Examiner argued that the tungsten plug is not shown. Applicant has modified Fig. 15 to point out some of the plug formations. Additionally, it is not necessary to show an M2 layer because the presence of "M1" implies additional layers; otherwise if "M1" were only one layer, it would be expressed simply as "M" instead of "M1". Applicant has, however, modified Fig. 15, to show M2. Applicant therefore asserts that this issue has now been removed. Regarding Fig. 17, the Examiner stated that it is not clear what RPO means. Applicant has modified Fig. 17 to remove RPO from Fig. 17. Applicant therefore asserts that this issue has now been removed.

In summary, Applicant asserts that the issue of the drawings in totality has also been removed. Applicant therefore respectfully requests that the objection to the drawings being withdrawn because the drawings have now been corrected and discrepancies thereof clarified herein.

II. Specification

The Examiner stated that 35 U.S.C. 112, first paragraph, requires that the specification be written in "full, clear, concise and exact terms." The Examiner argued that the specification includes terms, which are not clear, concise and exact. The Examiner indicated that the specification should be revised in order to comply with 35 U.S.C. 112. The Examiner stated that some of the examples of non-compliance o f the specification was cited in the office action of April 1, 2003.

The Examiner cited, as examples, of such non-compliance under 35 U.S.C. 112, first, paragraph, the following:

On page 12, paragraph 38, the Examiner indicated that salicide gate is disclosed without steps for the formation of the salicide gate. The Examiner indicated that the specification stated that "SAC may be configured for use with the semiconductor step" without steps for forming or description as to how the SAC

may be configured. The Applicant respectfully disagrees with this assessment. The statement "SAC may be configured for use with the semiconductor step" satisfies the formation of the salicide gate. The phrase "configured" in and of itself is a formation or creation step. When an item or thing is "configured," it is formed or created. The Applicant submits that one skilled in the art would have sufficient enablement and teaching via the phrase "SAC may be configured for use with the semiconductor step" in order to form a salicide gate thereof.

The Examiner further indicated that "Combining, the self-aligned contact and the salicide gate in the same cell area can effectively reduce gate resistance" is recited without any description of the method as to how the combination is achieved. The Applicant respectfully disagrees with this assessment. The sentence "Combining, the self-aligned contact and the salicide gate in the same area" in and of itself is sufficient to enable one skilled in the art to practice that particular step. The self-aligned contact and salicide gate can be combined in the same cell area to reduce gate resistance. The Applicant believes that it is not necessary to provide any further description of such a combining step, because that particular statement is sufficient in and of itself to enable one skilled in the art to understand clearly and concisely what must happen, i.e., the self-aligned contact and salicide gate can be combined in the same cell area.

The Examiner argued that on page 14, paragraph 40, the recitation that a "poly gate is defined" does not describe how the gate is defined and does not point out the gate. The Applicant respectfully disagrees with this assessment. The term "defined" does not mean that the poly gate is actually formed, only that the poly gate is being "set up" or defined for the formation. The poly gate is formed to include poly plugs 34, 36 and 38. Although the poly gate may not actually be shown in a particular step, it is important to realize, as indicated in the specification, that "in FIGS. 1 to 15 herein, analogous parts are indicated by identical reference numerals" and that "FIGS. 1 to 15 together represent a semiconductor fabrication

process that may be implemented in accordance with a preferred or alternative embodiments of the present invention." Thus, for example, with reference to all of the Applicant's figures in their entirety, one skilled in the art would recognize the formation and/or definition of a poly gate or other features and thus it is not necessary to point out the poly gate because the figures in and of themselves. For example, a poly gate should include poly plugs 34, 36, and 38, which are shown in the various figures.

The Examiner argued that on page 14, paragraph 41, it is stated that "third step 14 illustrates plug implant" and that there is not a description of a plug implant and no indication of a plug implant in the figure. The Applicant respectfully disagrees with this assessment. FIG. 3 of Applicant's specification shows poly plugs 34, 36, and 38 which are plug implants. Thus, a description of a plug implant is shown in the specification and one or more of the figures, which as indicated above, are to be interpreted together in their entirety, rather than as individual distinct inventions.

The Examiner argued that on page 15, paragraph 43, the recitation "involves an oxide/silicon nitride etch back step" does not explain how an oxide/silicon nitride etch back step is involved in the process. The Applicant respectfully disagrees with this assessment. An "etch back step" is a standard step in semiconductor processes. Thus, the use of the term oxide/silicon nitride etch back step is sufficient in and of itself as a clear and concise description of a desired step to be performed as part of the inventive process described in the specification.

The Examiner additionally argued that on page 15, paragraph 43, "LDD implant 50 layer is deposited" is not clear how implantation and deposition can be done and appears to be contradictory. The Applicant respectfully disagrees wit h this assessment. The term "deposited" refers to a "deposition" step. It is not necessary to explain in further detail how a deposition can be performed, because

the term deposition or deposited is a well known term to those skilled in the art. Thus, the Applicant submits that the phrase "LDD implant 50 layer is deposited" is sufficient, because it is a clear and concise explanation and the term "deposited" speaks for itself. Additionally, the Examiner has not explained how the use of "LDD implant layer" is contradictory, and if so, why this does or does not enable the claims and adds or subtracts from the inventive processes disclosed in Applicant's claims and specification.

The Examiner further stated that the specification is replete with undefined acronyms like "RPO" on page 17 and requested appropriate corrections. The Applicant respectfully disagrees with this assessment. The Applicant has amended the specification previously as indicated herein to remove the term "RPO." In addition, the Applicant points out that many of the acronyms are adequately defined in the specification. For example, LDD is defined as "lightly doped drain," TEOS is defined as Tetraethoxysilane, and so forth.

Additionally, Applicant reminds the Examiner that the specification, drawings, background and so forth are utilized to comply with 35 U.S.C. 112, and that the Examiner must not merely look toward specific examples of non-compliance thereof, but must consider the entire specification as a whole, including the drawings and the specification, and so forth, in order to set forth a rejection under 35 U.S.C. 112. Applicant believes that the specification as a whole satisfies the requirements of 35 U.S.C. 112. Applicant also reminds the Examiner that the claims can also enable the application. In other words, the claims form part of the specification, therefore the claims themselves can also be utilized for enablement of the application as a whole. Applicant therefore submits that the specification is written in full, clear, concise and exact terminology and therefore complies with the requirements of 35 U.S.C. 112.

III. Claim Rejections Under 35 U.S.C. § 112

The Examiner rejected claims 1-28 under 35 U.S.C., first paragraph, as failing to comply with the enablement requirement. The Examiner argued that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most clearly connected, to make and/or use the invention.

The Examiner argued that in claims 1 and 14, the method of fabricating the MIM capacitor and self-aligned contact is not described in the specification in such a manner as to enable a person of ordinary skill in the art to make and/or use the invention. The Examiner argued that regarding claim 1, combining of salicide date and self aligned contact in a memory cell area is not described in the specification as to enable a person of ordinary skill in the art to make and/or use the invention. Regarding claim 14, the Examiner argued that fabricating an MIM capacitor is not described in the specification in such a manner as to enable a person of ordinary skill in the art to make and/or use the invention. The Examiner argued that formation of the dielectric of the MIM capacitor and the formation of the metal-two is not described in the specification in such a manner as to enable one of ordinary skill in the art to make and/or use the invention. Applicant respectfully disagrees with this assessment.

Combining of salicide date and self aligned contact in a memory cell area is described in the specification as to enable a person of ordinary skill in the art to make and/or use the invention. For example, Figs. 1-17, including the flow chart teach clearly combining of salicide date and self aligned contact in a memory cell area. Figs. 1-17, the detailed description section, and the claims also disclose fabricating an MIM capacitor in such a manner as to enable a person of ordinary skill in the art to make and/or use the invention. The claims themselves are considered part of the specification, and the steps claimed are described by the claims themselves. Therefore, in addition to the drawings and text (e.g., detailed

description), the claims also provide sufficient disclosure to enable a person of ordinary skill in the art to make and/or use the invention.

Regarding claims 15 and 28, the Examiner argued that the system for fabricating an MIM capacitor is not described in the specification in such a manner as to enable a person of ordinary skill in the art to make and/or use the invention. The Examiner argued that claims 15-28 lack method system for fabricating an MIM capacitor. The Applicant respectfully disagrees with this assessment. Again, Examiner should look at the entire detailed description, drawings, flow charts, and the claims to conclude that a person of ordinary skill in the art can make and/or use the invention based on the claims, detailed description, drawings, etc. A complete method and system for fabricating an MIM capacitor is shown in detail in the drawings, the flow chart, the claims and the detailed description. Additionally, The claims themselves are considered part of the specification, and the steps claimed are described by the claims themselves. Therefore, in addition to the drawings and text (e.g., detailed description), the claims also provide sufficient disclosure to enable a person of ordinary skill in the art to make and/or use the invention. The claims clearly provide various method steps (in detail) for fabricating an MIM capacitor.

Applicant therefore believes that the rejection to claims 1-28 under 35 U.S.C. 112, first paragraph, has been traversed and therefore the rejection should be withdrawn.

IV. Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1, 2 and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Huang et al, "Huang", (U.S. Patent No. 6,146,941) in view of S. Wolf, "Wolf" (Silicon Processing for the VLSI Era, Volume 2, Pages 144-152). Regarding claims 1 and 2, the Examiner argued that Huang discloses, in columns 4-6 and in Figs. 2A-2F, a method of fabricating a capacitor formed on a substrate

wherein the capacitor is used in a semiconductor device comprising the following steps: designating and patterning a gate comprising polysilicon (206) for the semiconductor device; patterning configuring a self-aligned contact and performing an implant, in column 5 and lines 1-28, for the semiconductor device and; combining the gate and SAC in a memory cell area of the semiconductor device, in column 4, and lines 65-66. The Examiner admitted, however, that Huang lacks a salicide gate.

The Examiner argued that Wolf teaches in Figs. 3-39 on page 145 salicide gate processing steps along with SAC. The Examiner therefore argued that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Huang et al with that of Wolf to fabricate a capacitor in a semiconductor device with a low contact resistance and to increase memory cell density. The Applicants respectfully disagree with this assessment because the ability to create low contact resistance and to increase memory cell density is not disclosed, taught or suggested by either Wolf or Huang. The Examiner has not identified which portions of Huang and/or Wolf suggest creating low contact resistance while also increasing memory cell density. The Examiner has also not provided a reasonable explanation of why one skilled in the art would have been motivated to have combined Huang with Wolf to create low contact resistance and to increase memory cell density.

The Applicants remind the Examiner that the references may not be taken out of context and combined without motivation, in effect producing the words of the claims (and sometimes, not even the words or concepts of the claims), without their meaning or context. The resultant combination would not yield the invention as claimed. The claims are rejected under 35 U.S.C. 103 and no showing has been made to provide the motivation as to why one of skill in the art would be motivated to make such a combination, and further fails to provide the teachings necessary to fill the gaps in these references in order to yield the invention as claimed.

The rejection under 35 U.S.C. 103 has provided no more motivation than simply to point out the individual words of the Applicants' claims among the references, but without the reason and result as provided in the Applicants' claims and specification, and without reason as to why and how the references could provide the Applicants' invention as claimed. Hindsight cannot be the basis for motivation, which is not sufficient to meet the burden of sustaining a 35 U.S.C. 103 rejection.

Regarding claims 10-13, the Examiner rejected claims 10-13 as dependent upon claim 1. The Applicant submits that the arguments presented herein against the rejection to claims 1 and 2 under 35 U.S.C. 103 also apply equally to the rejection to claims 10-13.

Thus, claims 1, 2 and 10-13 of the present invention are not taught or suggested by Huang et al or Wolf, alone or in combination with one another. Combining these references fails to teach or yield the invention as claimed. The combination of these references fails to teach or suggest all the elements of the claims. Further, one of skill in the art would not be motivated to make such a combination. Therefore, the present invention is not obvious in light of any combination of Huang et al and/or Wolf. Withdrawal of the §103 rejections is therefore respectfully requested.

V. Allowable Subject Matter

The Examiner stated that claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant has therefore amended the claims so that claims 3-9 are now rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Claim 3 was previously dependent upon claim 2 which in turn

was dependent upon claim 1. All of the features of claims 2 and 3 have now been incorporated into claim 1 as amended herein. Similarly, claim 4 has been amended so that claim 4 now is rewritten in independent form and includes all of the limitations of claims 3, from which claim 4 was previously dependent and any base or intervening claims thereof (i.e., claims 1, 2, and 3).

Also, claim 5 was previously dependent upon claim 4, which in turn was dependent upon claim 3, and so on. Claim 5 has now been rewritten in independent form to include all of the features of the base claim and any intervening claims thereof (i.e., claims 1, 2, 3, and 4). Therefore, claim 5 is now also allowable because claim 5 has been rewritten in independent form per the Examiner's suggestions. Applicant therefore submits that because claim 5 is now allowable, any dependent claims thereof should also be allowed. Therefore, Applicant requests that claims 6, 7 and 8 also be allowed.

Additionally, claim 9 has been amended so that claim 9 is now rewritten in independent form and includes all of the limitations of the base claim and any intervening claims. To this end claims 10-13 have been amended so that claims 10-13 are now dependent upon claim 9. Because claim 9 is now in condition for allowance, Applicants believes that claims 10-13 should also be allowed.

III. Conclusion

In view of the foregoing discussion, Applicant has responded to each and every rejection of the Official Action, and respectfully request that a timely Notice of Allowance be issued. Applicant has clarified the structural distinctions of the present invention. Applicant respectfully submits that the foregoing discussion does not present new issues for consideration and that no new search is necessitated. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §112 and §103 and any objections to the drawings, and further examination of the present application.

Should there be any outstanding matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

Randy Tung (31,311)

Inventor: Min-Hsiung Chiang, et al.
Serial No.: 09/975,840 Filed: 10/11/2001
For: Methods And Systems For Forming Embedded DRAM For An MIM Capacitor
Attorney Doc. No.: 67,200-547

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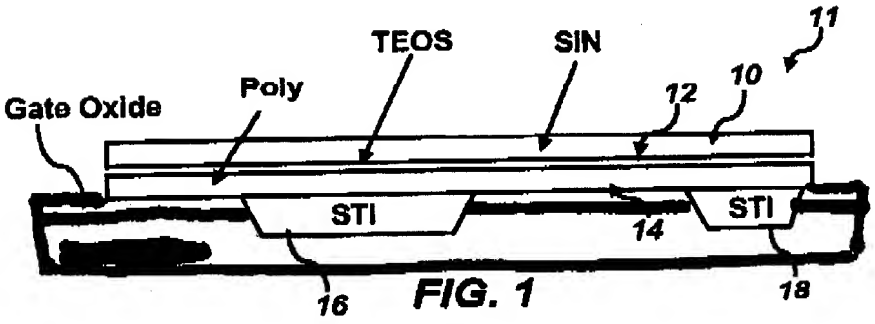

FIG. 1

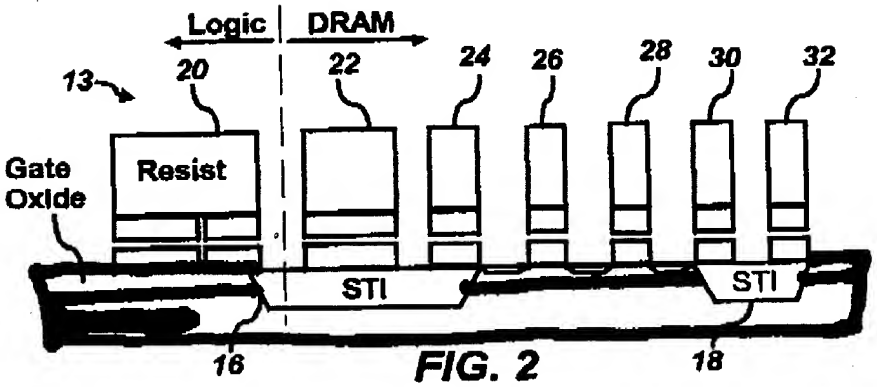

FIG. 2

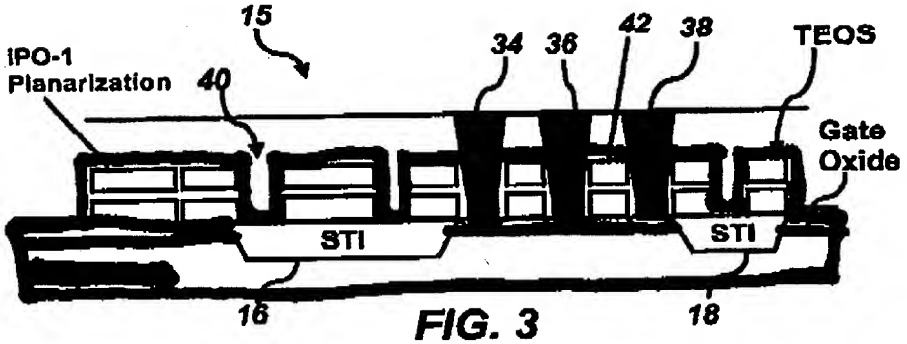

FIG. 3

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For: Methods And Systems For Forming Embedded DRAM For An MIM Capacitor
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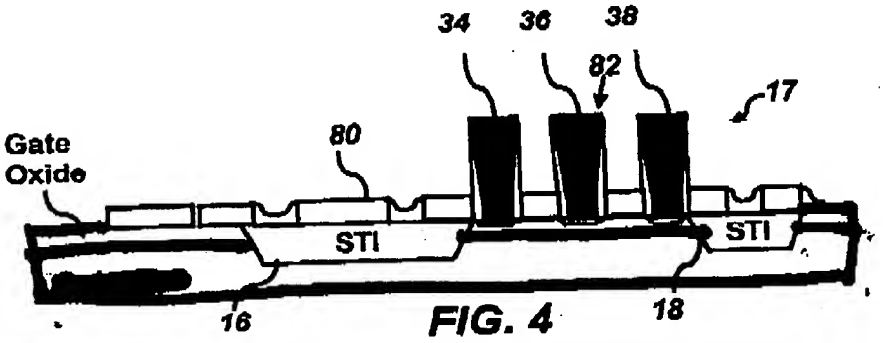

FIG. 4

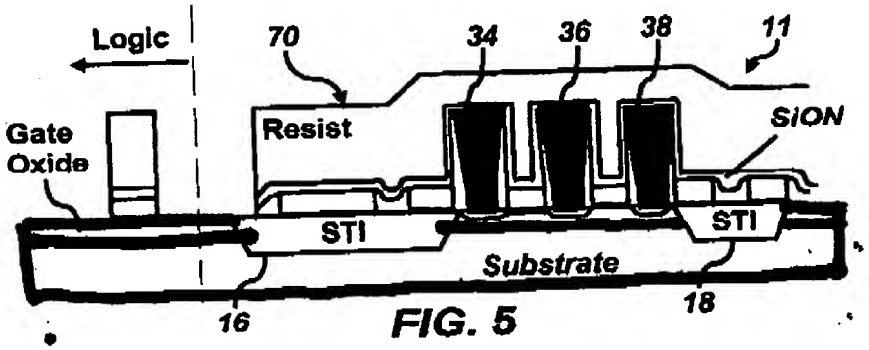

FIG. 5

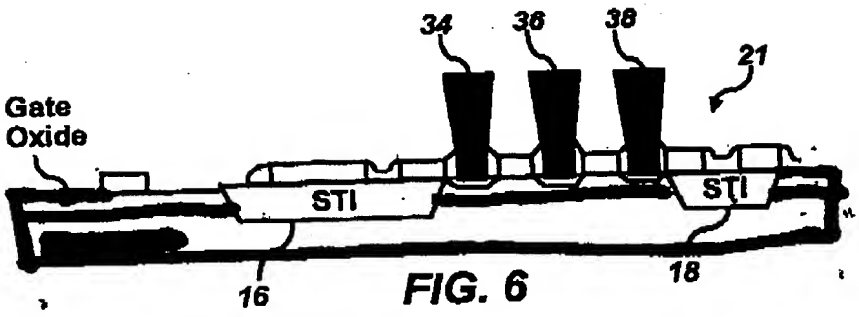

FIG. 6

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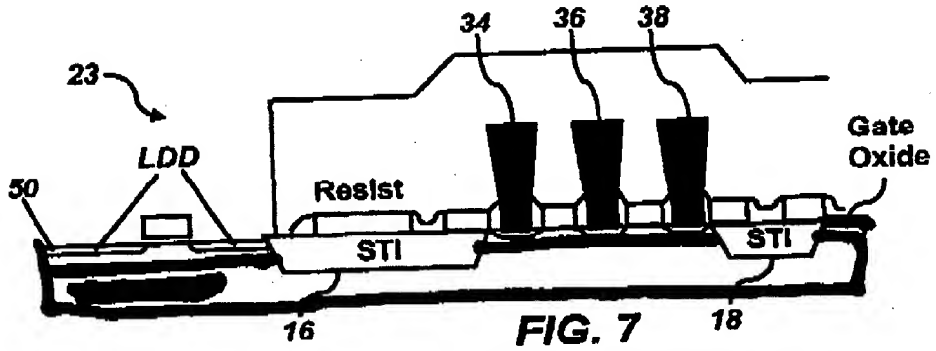

FIG. 7

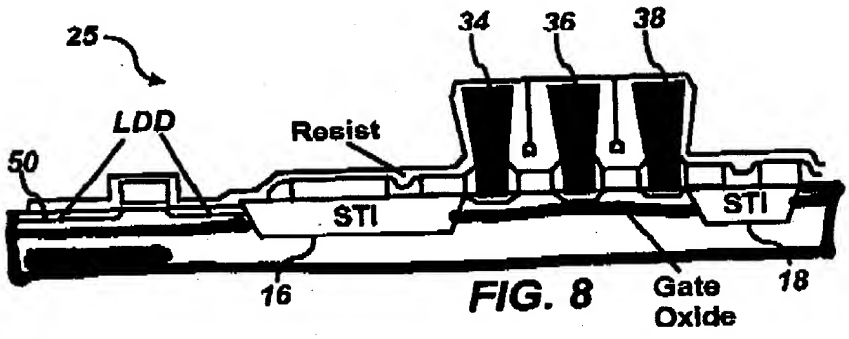

FIG. 8

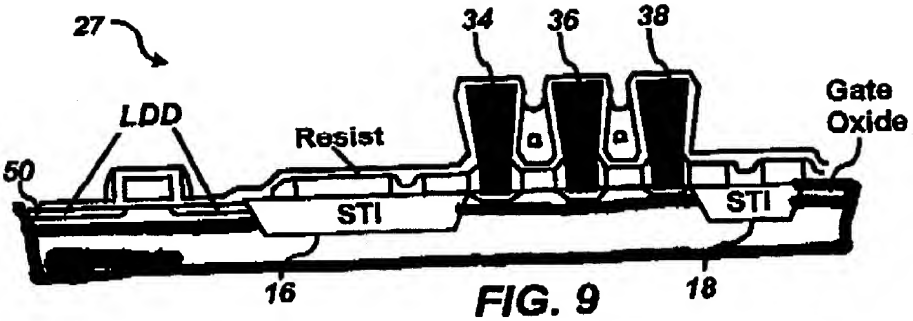

FIG. 9

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Attorney Doc. No.: 67,200-547

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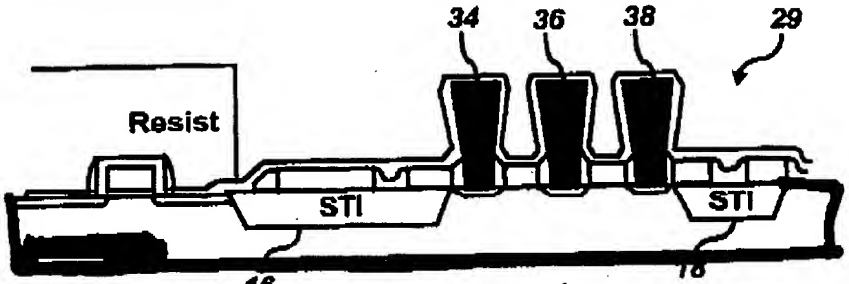

FIG. 10

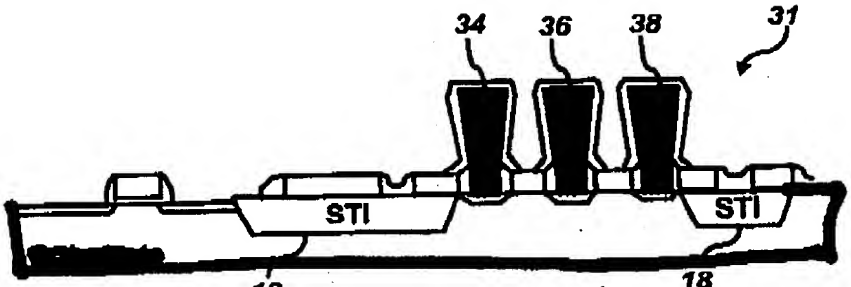

FIG. 11

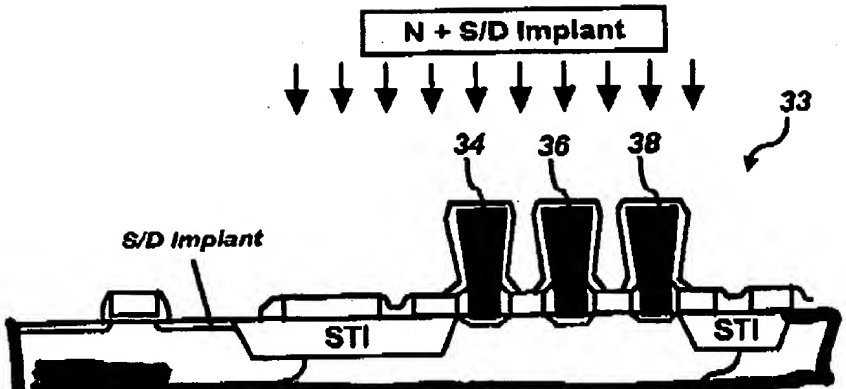

FIG. 12

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Attorney Doc. No.: 67,200-547

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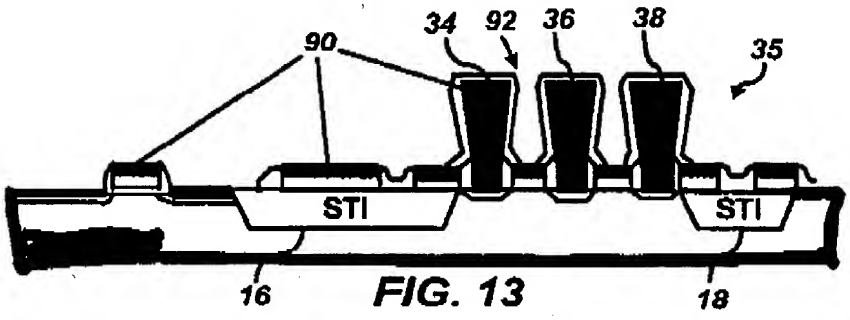

FIG. 13

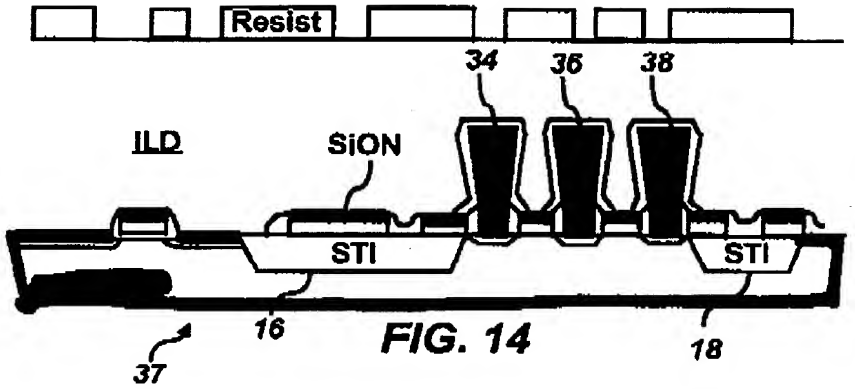

FIG. 14

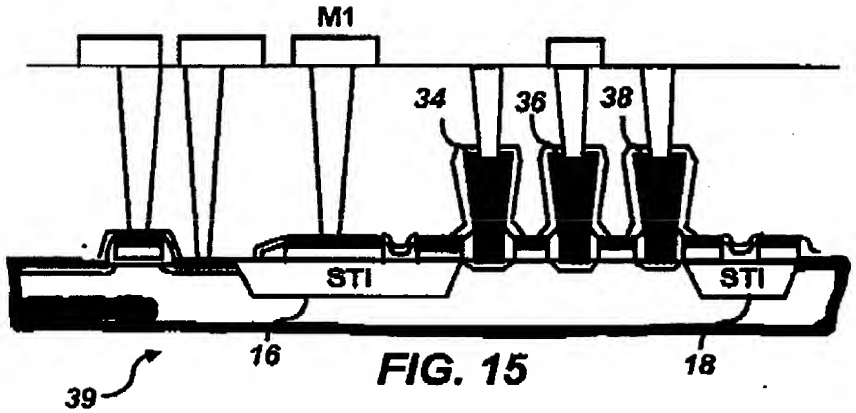

FIG. 15

Serial No.: 09/975,840 Filed: 10/11/2001
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Attorney Doc. No.: 67,200-547

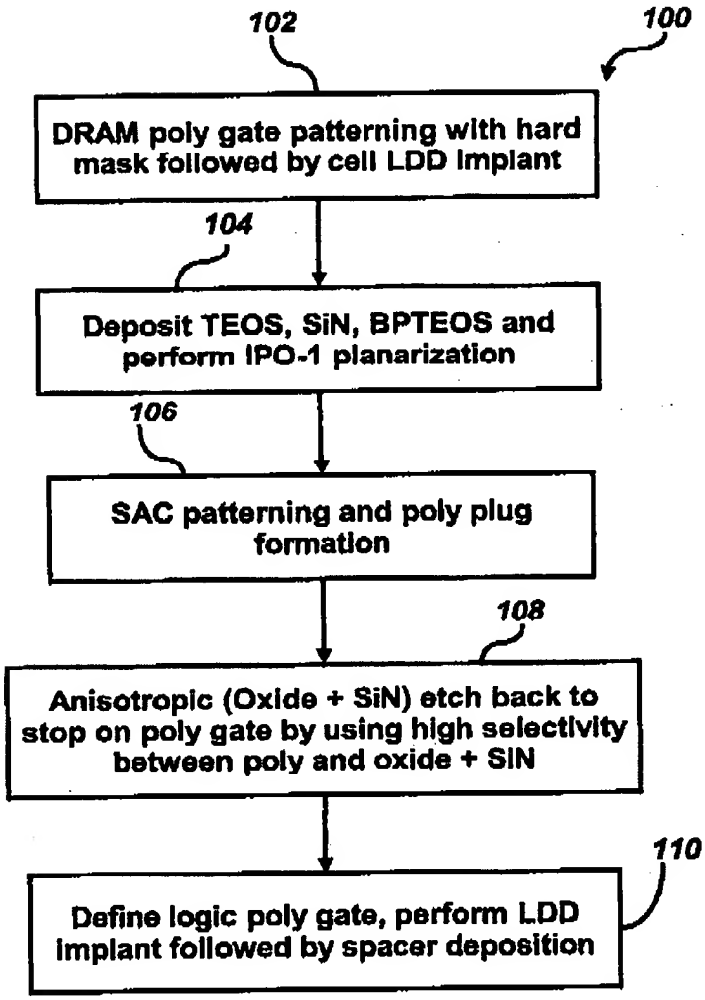

FIG. 16

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Attorney Doc. No.: 67,200-547

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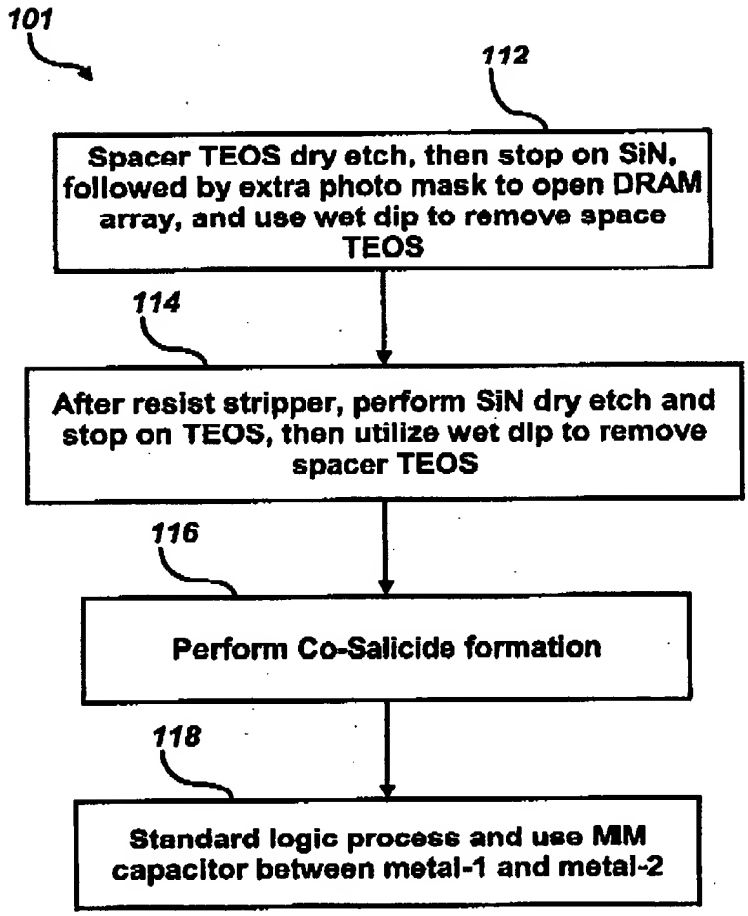

FIG. 17